

# INSTRUCTION MANUAL

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## CDB 5

1kHz CAPACITANCE DEVIATION BRIDGE

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A label consisting of a hexagon with a double border. Inside the hexagon, the words "SERIAL NO" are written in a sans-serif font.

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1. INTRODUCTION

The CDB 5 is a four-terminal capacitance deviation and loss-factor measuring system intended for high accuracy, high speed industrial use.

The four-terminal arrangement eliminates measuring errors due to lead impedance and contact resistance and makes it possible to measure a wide range of capacitance values with an accuracy of 0.1% or better simultaneously with a loss factor down to  $10^{-4}$  or better; at a measuring frequency of 1kHz.

The capacitance value is measured as a deviation (in %) from a built-in high accuracy four decade standard. The loss factor is measured directly in %.

The system consists of a main frame with a removable bridge module fitted in.

The main frame contains the digital meters, the limit detectors for sorting use, and the electronics for controlling the bridge functions.

The bridge module contains the bridge circuit, the measuring electronics, and the decade standard.

The main frame provides outputs of the measured parameters ( $\Delta C_s$  &  $\tan\delta$ ) both in analogue form for further limit selection and in parallel BCD code.

The measuring system is auto-balancing, which means a constant measuring voltage (within the selected range) and high speed.

## SECTION 1

## SPECIFICATIONS

MEASURING FREQUENCY	1kHz $\pm$ 0.1%
RANGE	10pF - 1111 $\mu$ F in 6 ranges
MEASURING VOLTAGE	3V RMS to 0.3 mV RMS
METERS	3 $\frac{1}{2}$ digit
RESOLUTION	$\Delta C_s$ 0-20%:0.01%( $10^{-4}$ ) 0-200%:0.1%( $10^{-3}$ )  $\tan\delta$ 0-2%:0.001%( $10^{-5}$ ) 0-20%:0.01%( $10^{-4}$ ) 0-100%:0.1%( $10^{-3}$ )
ACCURACY (incl. standard)	1nF to 10 $\mu$ F $C_s$ : $\pm$ 0.1% $\pm$ 0.1% $\times$ $\Delta C$ $\pm$ 1 digit $\tan\delta$ ( $\Delta C_s < 2\%$ ): $\pm$ 0.01% absolute, $\pm$ 1% of reading $\pm$ 1 digit  INACCURACY TO BE ADDED: 100pF to 1nF $C_s$ $\pm$ 0.1% $\tan\delta$ $\pm$ 0.04% absolute  10 $\mu$ F to 100 $\mu$ F $C_s$ $\pm$ 0.2% $\tan\delta$ $\pm$ 0.1%  100 $\mu$ F to 1000 $\mu$ F $C_s$ $\pm$ 1% $\tan\delta$ $\pm$ 0.5%

## SECTION 1

## SPECIFICATIONS

SETTLING TIME	Max, 150 msec for all C-values
STANDARD	3 decades + calibrated continuous variable, capacitor
OFFSET ADJUSTMENT	Compensate for stray capacitance and parallel conductance of test fixture
LIMITS	Adjustable limits with LOW/PASS/HIGH indication for $C_s$ and ACCEPT/REJECT indication for $\tan\delta$ . Limit settings are indicated on the display
OUTPUTS	Analog 10Vf.s. and parallel BCD output, $\Delta C_s$ and $\tan\delta$ . Limit output.
OUTPUT LEVEL	TTL
MAINTENANCE	Built-in test features for maintenance requiring a minimum of service equipment
CABINET	19" rack
DIMENSIONS	Height: 192 mm Width: 484 mm Depth: 356 mm
WEIGHT	11 kg
OPTIONS	4-terminal test-jig connected to front panel with coax cables. Cable length 1 meter. Memory for Limit Output

2. OPERATING INSTRUCTIONS2.1. Setting Up  
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Check that the mains voltage selector on the rear panel is set to the actual supply voltage.

To change the setting pull the knob, turn to the correct position and push back.

Check that a 0.5A slow-blow fuse, housed in the mains input socket, is fitted.

Connect a test fixture (test jig) to the BNC socket connectors on the front panel of the bridge module with coaxial cables.

As a four-terminal bridge circuit is used, the two detector terminals (DET and BAL) and the two generator terminals (GEN and REF) respectively must be interconnected before any checks or measurements are possible.

Note that from the point where the interconnections are made the circuit becomes two-terminal.

Ideally, the interconnections should be made through the leads of the capacitor under test to make true four-terminal or Kelvin contacts.

If the test fixture is not self-shorting when no capacitor is in place, external shortings must be made when checking the bridge. Make sure that the shorting do not add extra capacitance across the fixture as the zeroing adjustment would then be faulty.

## 2.2. Initial Calibration

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At the Main Frame:

Set the  $\Delta C_s$  meter range at 10% f.s. and the  $\tan \delta$  meter range at 1% f.s.

At the Bridge Module:

Set the range switch at .1nF and the decade standard at zero

Switch on the bridge and allow for at least 30 minutes stabilization before calibration.

When the bridge is switched on it automatically goes in CHECK I mode as indicated by the yellow LED on the front panel of the module.

In this mode the measuring electronics is isolated from the bridge circuit and can be separately adjusted.

Push the 'Con't reading' button on the main frame to get the meters free-running.

Adjust  $\tan \delta_o$  trim potentiometer on the bridge module to zero reading on the  $\tan \delta$  meter.

The  $\Delta C_s$  circuit should not normally need zeroing wherefore no external means of adjustment is available. In case of a non-zero reading on the  $\Delta C_s$  meter in CHECK I mode follow the instructions in the maintenance section (4) of this manual.

Push the CHECK II button on the bridge module.

In CHECK II mode the bridge circuit is connected to the measuring circuit in a way that shows small bridge imbalances with high sensitivity. This makes it possible to trim out the zero or self capacitance and conductance of the test fixture.

Make sure that the standard decade is set to precisely zero.

Adjust the  $C_0$  and  $R_0$  trim potentiometers on the bridge module to zero reading on the  $\Delta C_s$  and  $\tan\delta$  meters respectively.

Place a low-loss capacitor of known value f.ex. a 20nF polystyrene on the test fixture and set the range selector for .1nF and the standard decades to x200.0.

Press the 'AUTO' and Con't reading' buttons on the main frame.

Now vary the decade standard setting to give a  $\Delta C_s$  reading of say  $\pm 10\%$  and observe the  $\tan\delta$  reading. Adjust the  $\tan\delta/\Delta C_s$  trim potentiometer on the bridge module front panel for constant  $\tan\delta$  reading (within 0.002%) when  $\Delta C_s$  varies.

### 2.3. Measurements

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#### 2.3.1. Measurement by Balancing

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Place the unknown (or a standard for test purpose) on the test jig.

On the Bridge Module:

Set the Range Selector on the lowest range consistent with the assumed value of the unknown in order to bring in as much of the standard decade as possible.

On the Main Frame:

$\Delta C_s$  f.s. 100%

$\tan\delta$  f.s. 100%

Push the 'AUTO' button on the main frame, the 'measure' LED should go on.

Push the 'Con't reading'.

Adjust the standard decades to zero reading on the  $\Delta C_s$  meter.

Switch to  $10\Delta C_s$  f.s. reading to obtain precise balancing.

If the standard can be set to ten times the present setting the next lower range on the range selector (if possible) should be selected and the standard adjusted accordingly. This ensures the most precise measurement with least noise.

The capacitance value is now obtained by the standard decade reading multiplied by the range selector reading.

Switch the  $\tan\delta$  meter f.s. to lowest possible setting to obtain direct reading of loss factor.

An out-of-range condition is indicated by the 'Accept' and 'Reject' limit indicators simultaneously going on.

#### 2.3.2. Deviation Measurement

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To measure an unknown capacitor's deviation from a nominal value set as follows:

Multiplier and standard dials to nominal value,  $\Delta C_s$  and  $\tan\delta$  meter f.s. switches to appropriate full scale values of expected maximum deviation and loss.

Place the unknown capacitor on the test fixture.

##### a. Continuous Mode:

Push the 'AUTO' and 'Con't reading' button and the meters will take new readings at a rate of about eight per second.

b. Triggered Mode:

Push the 'Trig' button and the CHECK I button.

Now, whenever the bridge is triggered either by the 'Trig' button or by the parallel input to the rear panel socket, the bridge goes in 'Measure' mode (unless the unknown is out of range) and stays there for about 120-150msec. in order to give the bridge time to balance. At the end of this measuring period, readings are obtained and retained on the meters and the bridge reverts to CHECK I mode. (If, in automatic sorting applications, a control of the zeroing of the bridge's measuring circuit is wanted, one (and only one) reading in CHECK I can now be obtained by a signal (contact closure) to the rear panel socket pin in parallel with the CHECK I button).

c. Automatic Triggered Mode:

Push the 'Trig' button and then the 'AUTO' button.

The bridge is now permanently in 'Measure' mode (i.e. the bridge is constantly trying to balance) but the meters are not triggered and consequently retains the last measurement.

By applying a new unknown to the test fixture the bridge is automatically triggered by its balancing action and after a measuring period of about 120-150msec. displays a new reading on the meters.

This may be a practical mode in handsorting applications as no further actions by the operator than the application of the capacitors to the test fixture are required.

A new measurement period is started and a new reading obtained in this mode whenever the bridge is triggered.



### 2.3.3. Test Limits

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Low/Pass/High limits for  $\Delta C_s$  and an ACCEPT/REJECT limit for  $\tan\delta$  are provided for sorting purposes.

In order to set the limits, set the meter full scale ranges and press 'Con't reading'.

Then operate the spring-loaded switches labelled 'LIMIT SET' and adjust the limit potentiometers on the main frame front panel.

When the  $\Delta C_s$  'LIMIT SET' switch is pressed up the High limit setting is displayed on the  $\Delta C_s$  meter. When pressed down the Low limit setting is displayed.

The  $\tan\delta$  limit setting is displayed on the  $\tan\delta$  meter when the  $\tan\delta$  'LIMIT SET' is pressed down.

### 2.3.4. Measurement errors

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#### a. Low capacitance values.

The specified accuracy is valid at settings of the decade standard down to total dial readings of 100.0.

When lower settings are required e.g. when measuring capacitance values below 1nF on the lowest range the uncertainty of measurement will increase due to noise, and errors in the standard.

At 100pF, the inaccuracy for C is about  $\pm 0.20\%$  and for  $\tan\delta \pm 0.06\%$  absolute value.

at 10pF, the corresponding figures are  $\pm 2\%$  and  $\pm 1\%$ .

b. Lead resistance.

The four terminal circuit minimizes the effect of lead resistance on all but the highest capacitance ranges.

The following figures give information on the errors to be expected on the different ranges. .

On the three nF ranges a resistance of  $10\Omega$  in the most sensitive leads may cause errors of  $\tan\delta$  reading up to 0.01% absolute value.

On the  $\times 0.01 \mu\text{F}$  range the error may be up to 0.05%.

The  $\times 0.1 \mu\text{F}$  range will show the same error with  $1\Omega$ , and  $1\Omega$  on the  $\times 1\mu\text{F}$  range causes about 0.5% error on both  $\tan\delta$  and  $\Delta C$ .

### 3. PRINCIPLE OF OPERATION

#### 3.1. The Bridge System

##### ----- Diagrams

The bridge circuit is a ratio-transformer design with a calibrated variable decade capacitor  $C_N$  on the balancing arm.

The bridge signal supply is obtained from the oscillator in the measuring circuit via the power amplifier (IC10) and a coupling transformer (T6).

By varying the ratio of the bridge transformer (T1) different signal amplitudes are applied to the unknown capacitor and the standard whereby the six ranges of the bridge are obtained.

When the capacitor being measured has a capacitance value exactly proportional to the set standard capacitor with the chosen ratio setting as the proportional factor, no signal will exist at the junction point between the two capacitors, i.e. the detector point. The currents through the two capacitors are exactly equal.

This situation exists whenever the bridge is balanced by adjusting the standard capacitor as described in paragraph 2.3.1.

When making deviation measurements (as in paragraph 2.3.2.) the bridge circuit will usually not be physically balanced, and the signal currents through the capacitors would be unequal but for the action of the automatic balancing system.

This acts by sensing the current difference at the detection point and then generate a balancing signal which is added across the standard capacitor in a negative feed-back fashion.

The current imbalance in the capacitors is thus reduced to a minimum determined by the gain of the balancing loop.

The balancing signal is coupled into the bridge circuit via the transformer T5 and added to the signal across the standard through the corresponding side of the ratio transformer.

As the total bridge voltage will vary with the degree of imbalance, the balance signal is also added to the oscillator signal, keeping this constant at the power amplifier input.

Several compensating circuits essential to the accuracy of the bridge are incorporated in the bridge circuit and will be described under section 4 of this manual.

### 3.2. The Measuring System

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#### 3.2.1. The Oscillator Loop (IC 11, 15, 20, 21, and 10)

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The oscillator (IC21), which supplies the bridge circuit, is amplitude controlled by feed back derived from the ratio transformer side connected to the capacitor being measured.

The signal amplitude across this capacitor (the 'unknown'), i.e. the measuring voltage, is thus kept constant within the chosen range. It varies with the range setting from .3mVrms on the highest range to 3Vrms on the two lowest in accordance with the ratio of the bridge transformer.

The feed-back signal is buffered through the reference amplifier, which supplies the whole bridge module with the 'Basic Reference Signal' (IC 11).

This signal is kept to a fixed amplitude (.3Vrms) by the amplitude detector (IC 15), which controls the oscillator.

### 3.2.2. The Detection System

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The detector amplifier (IC 22) sensing the current imbalance in the bridge arms is a low impedance input amplifier generating an output signal proportional to and exactly in phase with the imbalance current. The detector signal produced by a capacitance imbalance will thus be ninety degrees out of phase with the measuring voltage (and hence the 'Basic Reference Signal') because a current through a capacitor is  $90^\circ$  out of phase with the voltage across it. Consequently a loss factor imbalance will produce a detector signal in phase with Reference signal.

The detector signal is supplied to two amplitude detectors (the 'Main Detectors') in order to resolve the total imbalance signal into its capacitance and loss deviation parts.

The  $\Delta C$  Main detector (IC 23) must thus be referenced by a signal  $90^\circ$  out of phase with the Basic Reference, and the  $\tan \delta$  Main detector (IC 26) by a signal in phase with the Reference.

The reference signals are squarewaves derived from the Basic Reference Signal in the reference circuit described later (paragraph 3.3.).

The Main detector outputs, after further amplification, result in the  $V_o$  and  $V_t$  DC signals representing respectively the detected capacitance and loss imbalance.

$V_o$  and  $V_t$  drive the balance signal generating system (described in paragraph 3.4.).

The Balance signal is the vector sum of  $0^\circ$  and  $90^\circ$  signals precisely proportional in amplitude to  $V_o$  and  $V_t$  respectively.

The effective amplification factor from the Detector input to the Balance signal output (i.e. the open-loop gain of the auto balancing system) is high enough to make the residual error current into the detector input insignificant compared to the current through the unknown and the standard capacitors.

The Balance signal will thus always be 'right' and if the balance generating system is accurate, then  $V_o$  and  $V_t$  will be precise measures of the required capacitance and loss balancing signals applied to the bridge circuit.

$V_o$  and  $V_t$  are the measuring outputs from the Bridge module to the Main Frame. There, however, they require further manipulation in order to arrive at  $\Delta C_s$  and  $\tan\delta$  as  $V_t$  only represents the loss factor when  $V_o$  is zero. This is because it is the loss current which is balanced and the  $90^\circ$  balance signal put across the standard is thus forced to vary with the capacitance value or, in effect, with  $\Delta C$ .

$V_o$  does also require modification as it represents the deviation in equivalent series capacitance which is only equal to the other when  $\tan\delta$  is zero.

An analogue computer in the main frame transforms  $V_o$  and  $V_t$  to the appropriate values.

### 3.3. The Reference System

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The  $0^\circ$  and  $90^\circ$  squarewave reference signals for the main- and balance detectors are generated in a phase-locked loop (PLL) consisting of a voltage controlled squarewave oscillator (VCO IC 18) controlled by the output from a phase detector (IC 16/17) and a frequency divider (IC 19).

The VCO output is a 4kHz squarewave which is divided down to 1kHz by the fast schottky flip-flops in IC 19. This provides the four-phase squarewave reference signals ( $0^\circ$ ,  $90^\circ$ ,  $180^\circ$ , and  $270^\circ$ ) used by the various amplitude and phase detectors. The phase detector is referenced by the  $90^\circ$  (and  $270^\circ$ ) squarewaves and detects the phase difference between this and the Basic Reference, feeding an error current to the VCO.

The phase of the squarewave reference is thus locked firmly to the Basic Reference by the high gain of the PLL.

Small adjustments to this phase relationship can be made by the front panel potentiometer ' $\tan\delta/\Delta C$ ' which influence the off-set of the phase detector.

The denomination of this control reflects the fact that the  $\tan\delta$  reading will vary with the capacitive deviation if the reference phases are misadjusted to the bridge voltage phase.

The low rise- and fall times of the IC 19 ensures steep flanks and precisely 50% duty cycle of the squarewave signals necessary to minimize off-set errors in the detectors.

#### 3.4. The Balancing System

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This system consists of two branches generating the  $0^\circ$  and  $90^\circ$  components of the balancing signal.

The  $0^\circ$  branch is controlled by the  $V_o$  DC voltage and consists of voltage controlled amplifier (IC 35).

This amplifier is fed by the Basic Reference Signal and can supply a signal from max. amplitude ( $0^\circ$  phase) through zero to max. amplitude ( $180^\circ$ ) thus balancing  $\Delta C_s$ 's from +100% to -100%.

Its output is added to the  $90^\circ$  balancing signal in the output filter amplifier IC 36.

The  $90^\circ$  branch is much more complicated as it is designed as a loop with a high amount of feed-back.

The loop is driven by  $V_t$  through a gain compensating amplifier (in IC 31). The input of the loop is a virtual earth point where the driving current derived from  $V_t$  is balanced by a current proportional to the amplitude of the output  $90^\circ$  balancing signal component.

The  $90^\circ$  signal is generated by a voltage controlled amplifier (VCA) (IC 34) controlled by a high-gain DC amplifier (IC 32) at the input.

The VCA is supplied with a constant  $90^\circ$  signal derived from the Basic Reference by an integrating amplifier (IC 33).

The output signal of the VCA is fed to the output filter amplifier and there added to the  $0^\circ$  signal.

The total balance signal is fed back to a detector (IC 29/30) referenced by the  $90^\circ$  (and  $270^\circ$ ) reference signal.

The detector gives a DC output precisely proportional to the amplitude of the  $90^\circ$  component of the Balancing Signal, and feeds it back through a low-pass filter (IC 31) to the input of the  $90^\circ$  loop.

This phase selective feed-back serves two purposes.



First; ensures strict proportionality between  $V_t$  and the  $90^\circ$  component of the Balance signal owing to the high open-loop gain of the  $90^\circ$  loop and the good stability of the detector,

and second; it removes any phase errors in the  $0^\circ$  ( $\Delta C$ ) balancing signal which is very important as this signal is usually much the greater part of the Balance signal.

For instance, if we measure a  $\Delta C_s$  of 1% on a capacitor with  $\tan\delta$  of  $10^{-4}$  (a common enough situation) the  $\Delta C$  balancing signal ( $0^\circ$ ) will be a hundred times greater than the loss balancing ( $90^\circ$ ) signal and even small phase errors on the  $\Delta C$  signal would, if left uncorrected, be catastrophic for the accuracy of loss measurement.

### 3.5. The Main Frame System

#### 3.5.1. The Analogue Computer

The measured parameters  $V_o$  and  $V_t$  must be transformed to voltages representing the deviation in series capacitance and the loss factor ( $\tan\delta$ ).

A capacitor (at a given frequency) can be represented as a parallel and series combination with numerical values:

$$|Z_p| = \frac{X_p}{\sqrt{1+T^2}} \quad \text{where } X_p = \frac{1}{\omega C_p} \quad \text{and } T = \tan\delta$$

$$|Z_s| = X_s \sqrt{1+T^2} \quad \text{where } X_s = \frac{1}{\omega C_s}$$

For the same capacitor we have:  $|Z_p| = |Z_s|$  or

$$\frac{X_p}{\sqrt{1+T^2}} = X_s \sqrt{1+T^2} \quad \text{or} \quad C_s = (1+T^2) C_p \quad (1)$$

With the bridge in balance, i.e.  $\Delta C_p = 0$  and some loss in the unknown there clearly should be a  $\Delta C_s$  reading different from zero as  $C_s$  is different from  $C_p$  and the actual  $C_p$  value is shown on the standard decade ( $\Delta C_p = 0$ ); we have:

$$\Delta C_{s(T)} (\%) = \frac{C_p - C_s}{C_p} = \frac{C_p - (1+T^2) C_p}{C_p} = T^2 \quad \text{for } \Delta C_p = 0$$

Further, when the bridge is not in balance ( $\Delta C_p \neq 0$ ) we will have to add  $\Delta C_{s(\Delta C_p)} = (1+T^2) \Delta C_p$  from (1).

Consequently, the total  $\Delta C_s = \Delta C_{s(T)} + \Delta C_{s(\Delta C_p)}$  or

$$\Delta C_s = T^2 (1 + \Delta C_p) + \Delta C_p \quad (2)$$

We are measuring  $V_t$  and not  $T$ .  $T$  is derived from  $V_t$  (in %) by the formula

$$T = \frac{V_t}{1 + \Delta C_p} \quad (3)$$

because  $V_t$  represents the loss balancing voltage across the standard.

From (3) we get  $T^2 = \frac{V_t^2}{(1 + \Delta C_p)^2}$  and combined with (2) we arrive at  $\Delta C_s = V_t^2 \Delta C_p$  ( $= V_t^2 \Delta C_p + V_o$ , with  $V_o$  in %) (4).

An integrated multiplier (IC 61) coupled as a divider computes  $T$  from  $V_t$  (suitable scaled in a preamplifier IC 59) according to formula (3) and another multiplier (IC 60) computes  $\Delta C_s$  according to (4).

The outputs from the multipliers drive the meteramplifiers (IC 62 and IC 63).

As the digital panel meters have a greater range than the analogue circuits, three range limits (-100% and +120% for  $\Delta C_s$  and +100% for  $\tan\delta$ ) are incorporated (IC 56/57/58), which by switching on the LOW, PASS, and HIGH limit indicators for  $\Delta C_s$  simultaneously (or ACCEPT and REJECT for  $\tan\delta$ ) warns the operator of an out-of-range condition on either (or both) parameters.

Out-of-range signals are also available on the rear panel output socket.

#### 3.5.2. Limits

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LOW/PASS and PASS/HIGH limits for  $\Delta C_s$  and an ACCEPT/REJECT limit for  $\tan\delta$  are provided. They are set by front panel potentiometers on the respective meters with the help of the 'LIMIT SET' switches.

The limit sorting signals are available on the output socket along with a go/no go signal combining them all.

The signals can be delayed up to eight cycles for automatic sorting application, where the mechanical sorting operation is done down stream from the measuring position.

The delay is introduced simply by inserting three integrated circuits in prepared sockets and moving three straps.

#### 3.5.3. The Control System

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This digital (CMOS) circuit controls the modes and timing of the whole bridge according to the control inputs from the front panel switches. These are duplicated on the rear panel input socket where the active input signals should be contact closures (floating) between the relevant input and digital ground.

The length of the measuring period, i.e. the time between the triggering of the bridge setting it in measure mode and the triggering of digital meters is controlled by a resistor in the bridge module.

#### 4. MAINTENANCE INSTRUCTIONS

##### 4.1. The Front Panel Controls

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###### CHECK I.

When the CDB 5 is switched on, it enters the CHECK I mode, where the bridge circuit is separated from the electronics. In this mode the ' $\tan\delta_o$ ' is adjusted to zero reading on the  $\tan\delta$  meter (f.s. range 1%) whereby the zero off-set of the  $\tan\delta$  balancing loop is removed (allow for a suitable warm-up time ( $\sim 10$  min)). Push the 'Con't reading' button on the main frame for easy reading of the meters.

###### CHECK II

In this mode the bridge circuit is connected to the electronics in such a way that the bridge measures the  $\Delta C_p$  and  $G_p$  (parallel conductance) with greatly increased sensitivity. This makes it possible to accurately balance-out the capacitance and conductance of the measuring fixture or jig. The procedure is: After the CHECK I adjustment set the decade standard to zero and the range switch to the lowest range (.01nF).

Operate the CHECK II push button and adjust the ' $C_o$ ' and ' $R_o$ ' front panel potentiometers to a zero reading on both meters (lowest ranges).

Move the range switch to the highest range (1 $\mu$ F) and check that a zero reading is still obtained. Note that even very small off-sets on the standard decade air capacitor (lowest decade) will give no-zero readings on the  $\Delta C_s$  meter. If the reading is non-zero re-check  $\tan\delta_o$  in CHECK I. If the readings in CHECK II, top range are still not zero, the standard decade zero needs adjustment. Withdraw the bridge module from the main frame and readjust RV1302 and RV1024 (DWG 52232-2) ( $C_{NO}$  and  $R_{NO}$  respectively).

After that repeat the CHECK II (lowest range) adjustments of  $R_o$  and  $C_o$ .

#### 4.1.1. The $\Delta C_s$ Zero Adjustment

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In CHECK I only a  $\tan\delta$  zero control ( $\tan\delta_o$ ) is provided on the front panel as  $\Delta C_s$  normally does not exhibit noticeable drift. In case a small off-set on  $\Delta C_s$  has developed over a period of time (a large one would indicate a fault calling for repairs to be made) this can be put right by the following procedure extracted from the full maintenance instruction (paragraph 4.3.):

Withdraw the bridge module from the main frame and set CHECK I. In order to make sure that the observed off-set originates in the bridge module, switch down ( $\downarrow$ ) SW3503 and SW3103. (By 'switch down' or ' $\downarrow$ ' is meant: operate the test switch in question to a position of the knob closest to the front panel. The normal operating position of all the test switches on the PC boards is 'up' or ' $\uparrow$ ', i.e. with the knob farthest from the front panel). Thereby the  $\Delta C$  DC voltage ( $V_o$ ) and the  $\tan\delta$  DC voltage ( $V_t$ ) to the main frame are interrupted and replaced by ground. Both meters must now read zero (most sensitive meter range), otherwise some off-sets have developed in the main frame, which must be trimmed according to the maintenance instruction. (See below). If the main frame is O.k. reset ( $\uparrow$ ) SW3503 and SW3103 and proceed as follows for the  $\Delta C$  off-sets: Set SW2301  $\downarrow$  and set the range switch to range .1nF. Adjust RV2401 to lowest reading on the  $\Delta C_s$  meter (i.e. as close as possible to zero - there are some drift and a long time constant). Reset ( $\uparrow$ ) SW2301 and set SW3501  $\downarrow$ . Adjust RV3501 to zero  $\Delta C_s$  reading. Reset ( $\uparrow$ ) SW2301.

This C zeroing procedure should be done in CHECK I with the range switch in range .1nF and with the standard decade set to zero and no capacitor on the jig.

4.1.2. The  $\tan\delta$  Adjustment  
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For normal operation the  $\tan\delta$  procedure as described above suffices, but if more serious off-set on  $\tan\delta$  arises and f.ex. the ' $\tan\delta_o$ ' front panel potentiometer runs out of range, a more thorough adjustment is required; and the following procedure with the same conditions as mentioned for the  $\Delta C$  Zeroing, should be followed.

1. Set SW2602  $\downarrow$  and SW3101  $\downarrow$
2. Adjust RV2701 to Zero  $\tan\delta$  reading.
3. With the help of a Digital Voltmeter (DVM) connected to the right-hand end of R3034 (the 'long-legged' 261k $\Omega$  resistor to the right of IC30) adjust the  $\tan\delta_o$  front panel potentiometer to zero DVM reading. Connect the DVM to TP3101.
4. Set SW2901  $\downarrow$  and
5. Adjust RV3101 (take care; NOT RV2801) to Zero DVM reading.

NOTE: It is desirable with at least 10 $\mu$ V sensitivity on the DVM.

6. Reset ( $\uparrow$ ) SW2602 and adjust RV3201 to Zero  $\tan\delta$  meter reading.

NOTE: This adjustment is extremely sensitive and it might be necessary to switch to 100% f.s. meter range.

7. Reset ( $\uparrow$ ) SW2901 and SW3101 and the  $\tan\delta$  meter should read Zero (at 1% f.s.).

The last front panel control to be adjusted is the  $\tan\delta/\Delta Z$  trim potentiometer, which adjusts the relative phase of the reference squarewave in the measuring circuit to the bridge voltage. Apply a 10nF polystyrene capacitor with low, known  $\tan\delta$  ( $\sim 10^{-4}$ ) to the jig.

Set the range switch to .1nF and the standard decade to 100.0.

Push the 'AUTO' and 'CON'T READING' buttons on the Main Frame. Note the  $\tan\delta$  reading. The typical noise (flicker) on the  $\tan\delta$  will be  $2-3 \times 10^{-5}$  in balance. Vary the decade setting out to  $\pm 50\% \Delta C_s$  or more and adjust the  $\tan\delta/\Delta C$  potentiometer to constant  $\tan\delta$  reading over the whole  $\Delta C_s$  range. (Note that at high negative  $\Delta C_s$  deviation (increased decade setting) the flicker noise on the  $\tan\delta$  reading will increase).

At the best  $\tan\delta/\Delta C$  setting the mean  $\tan\delta$  reading should not vary more than about  $5 \times 10^{-5}$  over the whole  $\Delta C_s$  range ( $-100\%$  to  $+100\%$ ).

#### 4.2. The Main Frame Adjustment DWG No. 52231-2

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- a) The Main Frame contains the power supplies ( $\pm 15V$ ,  $+5V$ )
- b) The analogue circuits for computing the  $\Delta C_s$  value and the  $\tan\delta$  value from the  $V_o$  voltage (proportional to the  $\Delta C_p$  value) and the  $V_T$  voltage proportional to the actual loss balancing signal (IC59/60/61/62/ and 63).
- c) The range limits ( $-99\%$  and  $+120\%$  for  $\Delta C_s$ , and  $+100\%$  for  $\tan\delta$  or correspondingly less on the lower meter ranges). Exceeding the range limits is signalled by the simultaneous lighting up of all limit LED's for the offending parameter (IC56, 57, and 58).
- d) The sorting limits (IC53/54, and 55) are set by front panel potentiometers controlling test voltage generators (IC50/51, and 52) the output of which can be read directly on the meters by using the 'SET LIMIT' switches. Two of the test voltages TS1 (the  $\tan\delta$  Limit Voltage) and TS2 (the  $\Delta C$  LOW Limit Voltage) are also used for internal tests and adjustments purposes.
- e) The logic circuit which provides for timing and mode control of the bridge functions.



For maintenance adjustments of the Main Frame the following instrumentation are required:

A digital voltmeter (DVM) with at least  $10\mu\text{V}$  resolution, an oscilloscope, and a frequency (period) counter.

#### 4.2.1. Main Frame Adjustments - The Power Supplies

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The two power supply regulator boards are mounted in front of the mains transformer in the left of the cabinet, with the +5V regulator to the left. Of the two singleturn trimpotentiometers on the  $\pm 15\text{V}$  regulator the lefthand one sets both voltages and should be used to set the +15V. The right-hand one is then used to balance the -15V relative to +15V. All the supply voltages should be set to within 0.001V and after that they should not drift more than a few mV.

The test voltage generators IC50 and IC51 are controlled by the  $\tan\delta$  Limit - and the  $\Delta C_s$  LOW Limit potentiometers respectively, and the output voltages are named TS1 and TS2 and are present on the test points  $\text{TPTS}_1$  and  $\text{TPTS}_2$  situated to the left of the test generators. They can be seen as % limit values on the  $\tan\delta$  - and  $\Delta C$  meters respectively by using the LIMIT SET front panel switches.

TS1 is grounded by SW5002  $\downarrow$  and reduced to approx a tenth its set value by SW5001  $\downarrow$  (for better control of low voltage tests). Its normal ranges is  $\sim 0\text{V}$  to +10.1V.

TS2 is grounded by SW5102  $\downarrow$  and reduced to approx a tenth its set value by SW5101  $\downarrow$ . Its normal range is  $\sim +0.8\text{V}$  to -11V.

The TS2 can be extended by SW5103 to +10.1V to -10.1V.

TS1 and TS2 are routed to several points in the analogue circuit and through the flat cable to the bridge module where they can be used for test and adjustment purposes.

#### 4.2.2. The Digital Panel Meters

-----

The DPM's are selfcontained units supplied by 5V, using approx. 0.4A each.

Their inputs (200mV f.s. = 1999) are on the most right-hand pin in the upper row on the edge connectors.

The meters are tested by connecting the DVM to the input pin and applying a voltage to it by the appropriate LIMIT SET switch and test voltage. (Use TS1 = 10V and TS2 = -10V). The meters are equipped with adjustment potentiometers mounted behind the light filter front cover. Adjust them, if necessary, to correct reading (1000) with 100.00mV input.

#### 4.2.3. Adjustment of the Meter Dividers

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As the full scale output of the meter amplifiers ( $\Delta C_s$ :IC62 and  $\tan\delta$ :IC63) are 10.000V, resistive voltage dividers are at the inputs of the meters ( $\Delta C_s$  meter ip: R260-61-62, and RV6204;  $\tan\delta$  meter ip: R-6360-61-62, and RV6303).

1. Set TS1 to 10.000V with the DVM (on TPTS<sub>1</sub>) and connect the DVM to the  $\tan\delta$  meter ip pin on its edge connector.
2. Adjust RV6303 to exactly 100.00mV DVM reading.
3. Set TS2 to -10.000V with the DVM and connect the DVM to the  $\Delta C_s$  meter ip pin on its edge connector.
4. Adjust RV6204 to exactly 100.00mV DVM reading.

#### 4.2.4. The Analogue Computer (DWG Nos. 52231, -1, -2)

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This consists of the  $V_T$  preamplifier (IC59) and the two multipliers  $M_C$  (IC60) and  $M_T$  (IC61) driving the meter amplifiers: IC62 ( $\Delta C_s$ ) and IC63 ( $\tan\delta$ ) respectively.

$V_T$  is the DC voltage from the bridge circuit proportional to the loss balancing signal. At  $\Delta C_p = 0$  its scale is 50mV/%  $\tan\delta$  at 100% f.s. meter range ( $\tan\delta$ ), and 500mV/%  $\tan\delta$  at 10% and 1% f.s. meter range.

The  $V_T$  Amplifier gain is x0.5 for 10% and 100% meter f.s. and x5 for 1% meter f.s. The gain is controlled by the meter range switch through the reed relay REL5901. The  $V_T$  Amp is a LF356 (JFET input) selected to very low input off-set temperature drift ( $<3 \text{ V}/^\circ\text{C}$ ).

Adjustment of the  $V_T$  Amplifier (IC59):

1. Set SW5002  $\downarrow$  ( $TS_1 = \text{Zero (ground)}$ ).
2. Set SW5901  $\downarrow$  ( $TS_1$  instead of  $V_T$  into IC59)
3. DVM on TP5901 ( $V_T$  Amp output) and 1%  $\tan\delta$  meter f.s.
4. Adjust RV5901 to Zero DVM reading.
5. Reset SW5002  $\uparrow$  and set SW5001  $\downarrow$  (decreased  $TS_1$  range)
6. Adjust  $TS_1$  to +1.0000V with the DVM.
7. Set  $\tan\delta$  meter range to 1% and connect DVM to TP5901.
8. Adjust RV5902 to -5.000V DVM reading.
9. Set  $\tan\delta$  meter range to 10%.
10. Adjust RV5903 to -0.5000V DVM reading.

#### 4.2.5. The $M_T$ ( $\tan\delta$ ) Multiplier IC61

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$V_T$  is proportional to the loss balancing voltage in the bridge but this in turn, depends not only on the loss factor of the tested capacitor but also on its capacitance value relative to the standard, i.e.  $\Delta C_p$ .

Only when  $\Delta C_p$  is Zero will  $V_T$  and the true loss value  $V_{\tan\delta}$  be proportional.

$V_{\tan\delta}$  is derived from  $V_T$  and  $V_o$  (proportional to  $\Delta C_p$ ) by the  $M_T$  multiplier according to the formula  $V_{\tan\delta} = \frac{V_T}{1 + \Delta C_p}$  where  $\Delta C_p$  is normalized to  $V_o/V_o$  f.s.

$M_T$ , in effect, functions as a variable gain amplifier for  $V_T$ , with its gain (controlled by  $V_O$ ) ranging from  $x0.5$  to  $x\infty$  for  $\Delta C_p$  going from +100% to -100%.

For  $\Delta C_p$  close to -100% ( $V_O$  close to +10V) the gain of  $M_T$  becomes very high. At about -99% the  $\Delta C_s$  range limit LOW is crossed and applies a current to IC61 pin 10 through R6117 limiting the gain before the multiplexer is required to perform the impossible task of dividing by Zero!

Adjustment of  $M_T$ .

1. Set SW6102  $\downarrow$  (grounding TP5901).

NOTE: On CDB 5 with Serial Nos. 46684-46693, SW6102 & SW6101 have different functions from later instruments, in that the SW6101 selects between  $TS_1$  ( $\uparrow$ ) and  $TS_2$  ( $\downarrow$ ) and SW6102 replaces  $V_O$  with the selected TS. For these instruments point 1 must be replaced with: Remove IC5901 from its socket and short TP5901 with a short piece of wire to ground.

2. Set SW5002  $\downarrow$  and SW5102  $\downarrow$  ( $TS_1$  and  $TS_2$  ground).
3. Set SW6101  $\downarrow$  (and for Serial Nos. 46684-93: SW6102  $\downarrow$ )
4. Connect DVM to TP6101 ( $M_T$  output) and adjust RV6101 to Zero reading on DVM.
5. Connect DVM to wiper of RV6102 (or pin 10 on IC61) and adjust RV6102 to 5.000V reading on DVM.
6. Reset ( $\uparrow$ ) SW5102 ( $TS_2$  activated) and set SW5103  $\downarrow$  ( $-10V < TS_2 < +10V$ ).
7. Keep the  $\Delta C_s$  'LIMIT SET' front panel switch down in order to get an indication of  $TS_2$  on the  $\Delta C_s$  meter.
8. Adjust  $TS_2$  to near +100% reading on the  $\Delta C_s$  meter (i.e.  $TS_2$  near +10V. As  $TS_2$  is replacing  $V_O$  and  $V_O = 10V$  corresponds to  $\Delta C_p = -100\%$  we are in the high gain end of the  $M_T$  range where its off-set is most important. Do not be confused by the + set on  $\Delta C_s$  meter, it merely reflects the sign of  $TS_2$ ).

9. At about 99% the range limit is crossed (all three limit leds for  $\Delta C_s$  lights up). Adjust RV6101 to same reading on the DVM above and below the range limit.
10. Reset ( $\uparrow$ ) SW5001, SW5002, and SW5103 and set SW5102  $\downarrow$ .
11. Tan $\delta$  meter range switch: 100%.
12. Adjust TS<sub>1</sub> to +5.000V with DVM on TPTS<sub>1</sub> (on Serial Nos. 46684-93: remove the ground short on TP5901 and reinsert IC59 and let it stabilize).
13. Check with the DVM on TP5901 that the  $V_T$  Amp output is -2.500V (if not, the  $V_T$  Amp adjustment must be redone).
14. Connect the DVM to TP6101 and reset ( $\uparrow$ ) SW6102 (NOT on Serial Nos. 46684-93, where the  $V_T$  Amp output is permanently connected to the  $M_T$  input).
15. Adjust RV6102 to +5.000V reading on the DVM.

#### 4.2.6. The $M_C$ ( $\Delta C_s$ ) Multiplier IC 60

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As is well known the value of the equivalent series capacitance of a lossy capacitor is higher than the equivalent parallel capacitance at a given frequency. The formula is  $C_s = (1+T) C_p$ , where T is the loss factor in absolute value (1=100%). This is transformed for our use to  $\Delta C_s = V_T \times T + \Delta C_p$ , where  $V_T$  and  $\Delta C_p$  ( $V_o$ ) are measured values and T ( $V_{\tan\delta}$ ) developed by  $M_T$ . The integrated circuit multiplier, AD532, performs the calculation of  $V_{C_s}$  from these values. REL6001 & 5901 scales the  $V_T$  and T input according to the meter range setting of tan $\delta$ .

Adjustment of the  $\Delta C$  Multiplier  $M_C$  IC60:

1. Set SW5002  $\downarrow$ , SW5102  $\downarrow$ , and SW5103  $\uparrow$ .
2. Set SW6102  $\downarrow$  and SW6101  $\downarrow$ .
3. Connect the DVM to TP6001, the output of  $M_C$ , and measure the off-set voltage. This should be within  $\pm$  a few mV. In case IC60 has been replaced and the off-set exceeds say 3mV, R6101 must be adjusted in value to get the off-set within bounds.
4. Reset SW5102  $\uparrow$  and set TS<sub>2</sub> to -10.000V with the DVM connected to TPTS<sub>2</sub>.

5. Connect the DVM to TP6001 and adjust RV6001 to -2.500V DVM reading. If an off-set of say +1.0mV has been measured under point 3, the output should be set to -2.499V and for a measured off-set of -2.0mV the output should be set to -2.502V.

#### 4.2.7. The Meter Amplifiers. $\Delta C_s$ and $\tan\delta$

---

Both IC amps ( $\Delta C_s$ : LF356 and  $\tan\delta$ : LM301A) are selected to have  $T_C$  if the input off-set less than 7 V/ $^{\circ}$ C.

The  $\Delta C_s$  amp (IC62) has a gain of x4 for 100% f.s. meter range and x40 for 10% f.s. meter range. The gain is set by changing the feed-back through a section of the range switch.

The  $\tan\delta$  amp has a fixed gain x2.

The meter amp inputs are driven by the multipliers through SW6001 ( $\Delta C_s$ ) and SW6101 ( $\tan\delta$ ), which both selects  $TS_2$  when set down ( $\downarrow$ )

#### Adjustment of the $\Delta C_s$ Meter Amp

1. Set SW5102  $\downarrow$ , SW5101  $\downarrow$ , and SW5002  $\downarrow$  and connect the DVM to TP6201 ( $\Delta C_s$  meter amp output).
2. Set  $\Delta C_s$  meter range to 10%.
3. Set SW6101  $\downarrow$  and adjust RV6201 to Zero DVM reading.
4. Reset ( $\uparrow$ ) SW5102 and set  $TS_2$  to -0.2500V with the DVM connected to  $TPTS_2$ .
5. Connect the DVM to TP6201 and adjust RV6203 to +10.000V DVM reading.
6. Set  $\Delta C_s$  % f.s. to 100%.
7. Set SW5101  $\uparrow$  and set  $TS_2$  to -2.500V with DVM on  $TPTS_2$ .
8. Connect DVM to TP6201 and adjust RV6202 to +10.000V DVM reading.
9. Set SW5102  $\downarrow$  and SW6201  $\uparrow$ .
10. Set  $\Delta C_s$  % f.s. to 10% and readjust RV6201 to Zero DVM reading (this counters the residual off-set in the  $M_C$  in the most sensitive meter amp setting, i.e. x40 gain. The Zero fault at 100% (x4 gain) will then be too small to be observed on the meter).

Adjustment of the  $\tan\delta$  Meter Amp:

1. Set SW5002  $\downarrow$ , SW5102  $\downarrow$ , and SW6301  $\downarrow$ .
2. Connect the DVM to TP6301 (output of  $\tan\delta$  meter amp) and adjust RV6301 to Zero DVM reading.
3. Set SW5101  $\uparrow$  and SW5102  $\uparrow$  and set  $TS_2$  to -5.000V with the DVM on  $TPTS_2$ .
4. Connect the DVM to TP6301 and adjust RV6302 to +10.000V DVM reading.
5. (On instruments with Serial Nos. 46684-93: replace point 5 & 6 with the following:
  - a) Set SW6301  $\uparrow$ , SW5901  $\downarrow$ , SW5002  $\downarrow$ , and SW5102  $\downarrow$ .
  - b) Set  $\tan\delta\%$  f.s. to 1% and make sure with the DVM on TP5901 that the  $V_T$  amplifier (IC59) is properly zeroed. If not, readjust RV5901.
  - c) Connect the DVM to TP6302 and readjust RV6301 to Zero reading on the DVM).
 Set SW6301  $\uparrow$ , SW6102  $\downarrow$ , and SW5102  $\downarrow$ .
6. Readjust RV6301 to Zero reading on DVM (the off-set of  $M_T$  is absorbed by the  $\tan\delta$  meter apm).

## 4.2.8. The Range Limits

When the measured deviation exceeds certain limits the measurements are no longer guaranteed because of non-linearities and saturation of some circuits. The range limits are:

$\Delta C_s$  LOW RANGE LIMIT (IC56) -99%.

$\Delta C_s$  HIGH RANGE LIMIT (IC57) +120%.

$\tan\delta$  RANGE LIMIT (IC58) +100%.

When one of the range limits is passed, all the limit indicator LED's for that parameter will light up (i.e. when e.g. the  $\Delta C_s$  HIGH RANGE LIMIT is passed the LOW, PASS, and HIGH LED's will go on).

Adjust of the Range Limits.

The  $\Delta C_s$ :

1. Set SW5102  $\uparrow$ , SW5103  $\downarrow$ , and SW6201  $\downarrow$ .
2. Set  $\Delta C_s$  % f.s. range to 100% and  $\Delta C_s$  LIMIT SET Switch in mid position.
3. Set  $TS_2$  to -99.0% reading on the  $\Delta C_s$  meter and adjust RV5601 to the out-of-range indication just goes on.
4. Set  $TS_2$  to +120.0% reading on the  $\Delta C_s$  meter and adjust RV5701 to the out-of-range indication just goes on.

The  $\tan\delta$ :

5. Set SW6201  $\uparrow$ , SW6301  $\downarrow$ , and SW5103  $\downarrow$ .
6. Set  $\tan\delta$  % f.s. to 100%.
7. Set  $TS_2$  to +100% reading on the  $\tan\delta$  meter and adjust RV5801 to the out-of-range indication (ACCEPT and REJECT LED's both on) goes on.

#### 4.2.9. The Logic Circuit

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The Logic Circuit is designed with +15V CMOS IC's. The front panel push button signals arrives through R8017 (CHECK II), R8020 (CHECK I), R8021 (CON'T READING), R8023 (AUTO), and R8024 (TRIG) to the 'and' gates 14092<sub>I</sub> and 14081<sub>III</sub> which, in turn, controls the four mode flip-flop in 14044 circuit.

This controls through a further gate-network the three timers in the IC's 14528 I and II (the one-shot 14528<sub>I</sub> pin 9-16 is not used). The first timer (14528<sub>I</sub> p1-8) gives the  $Q_1$  positive (+15V) inputs, which is the cycle time of the measurement, i.e. the delay from the trig moment to the meters are triggered - a time necessary for the bridge circuit (and the analogue computer in the main frame) to settle so, that a stable (and correct)  $V_{\Delta C_s}$  and  $V_{\tan\delta}$  can be converted in the digital panel meters. This time is usually set to approx 150msec by C8006 and a resistor  $R_T$  located in the bridge module (to the right of the flat cable socket) approx 121k $\Omega$ . The measuring period can be varied by changing  $R_T$ , and the time be measured as the pulse length of  $Q_1$ , at test point TPQ<sub>1</sub>.

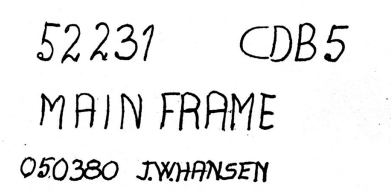


The falling edge of  $Q_1$  triggers  $Q_2$  ( $TPQ_2$ ), a 10 S, +15V positive pulse used to trigger the limit memory FF's (14013<sub>I</sub> & <sub>II</sub>) and, level shifted to 5V through 14049<sub>II</sub>, the digital panel meters (DPM's).

$Q_2$  triggers  $Q_3$ , a 10mS +15V pulse, inserted to allow the DPM's time to finish the conversions before the bridge can be retriggered or reverts to CHECK I states.

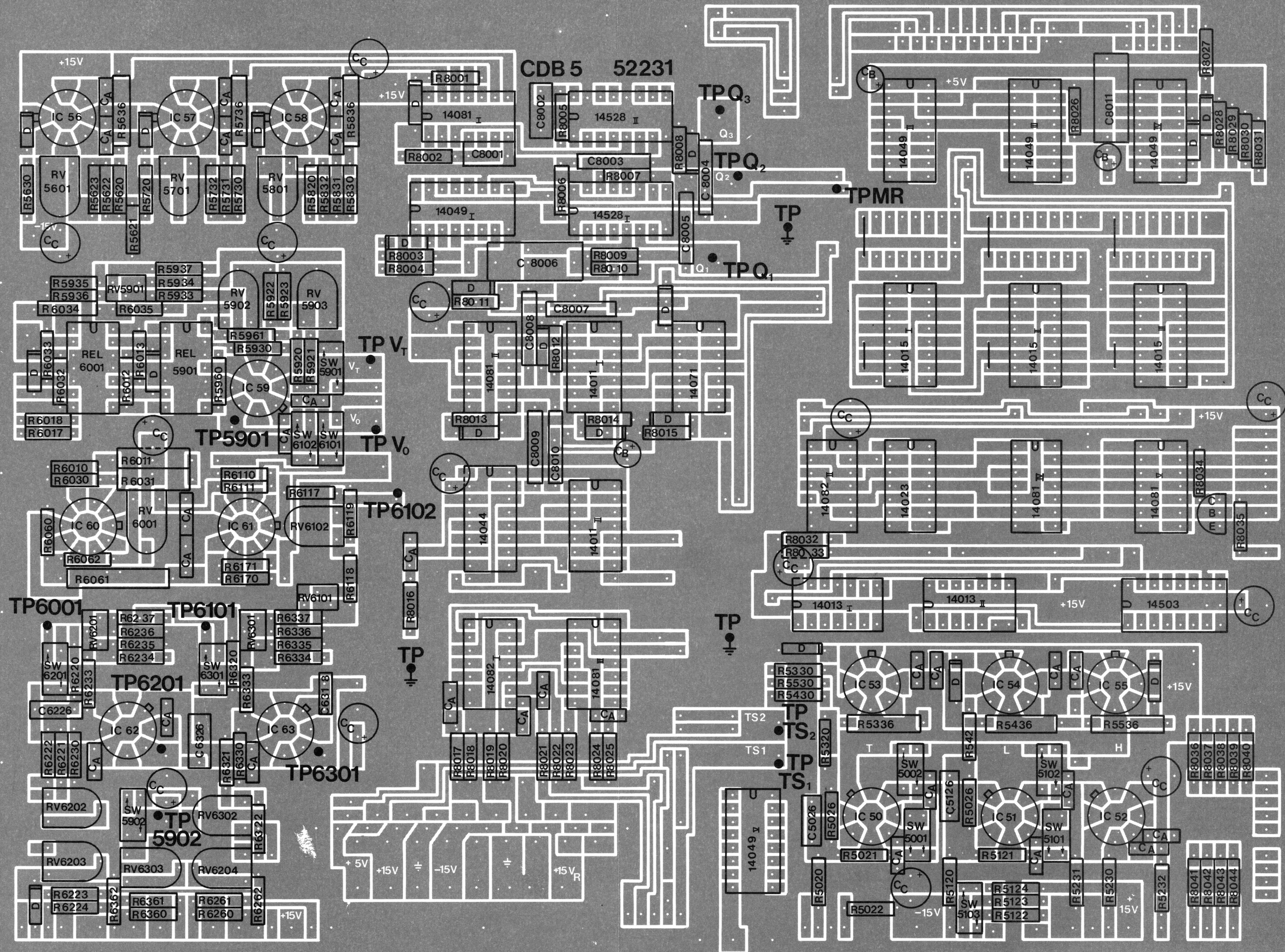
R8006 and C8003 sets the  $Q_2$  pulsetime and R8005 and C8002 sets the  $Q_3$  pulsetime.

NOTE: When finished with the circuit adjustment make sure that all test switches on the PCB are returned to their operating position which is  $\uparrow$  or away from the front panel.

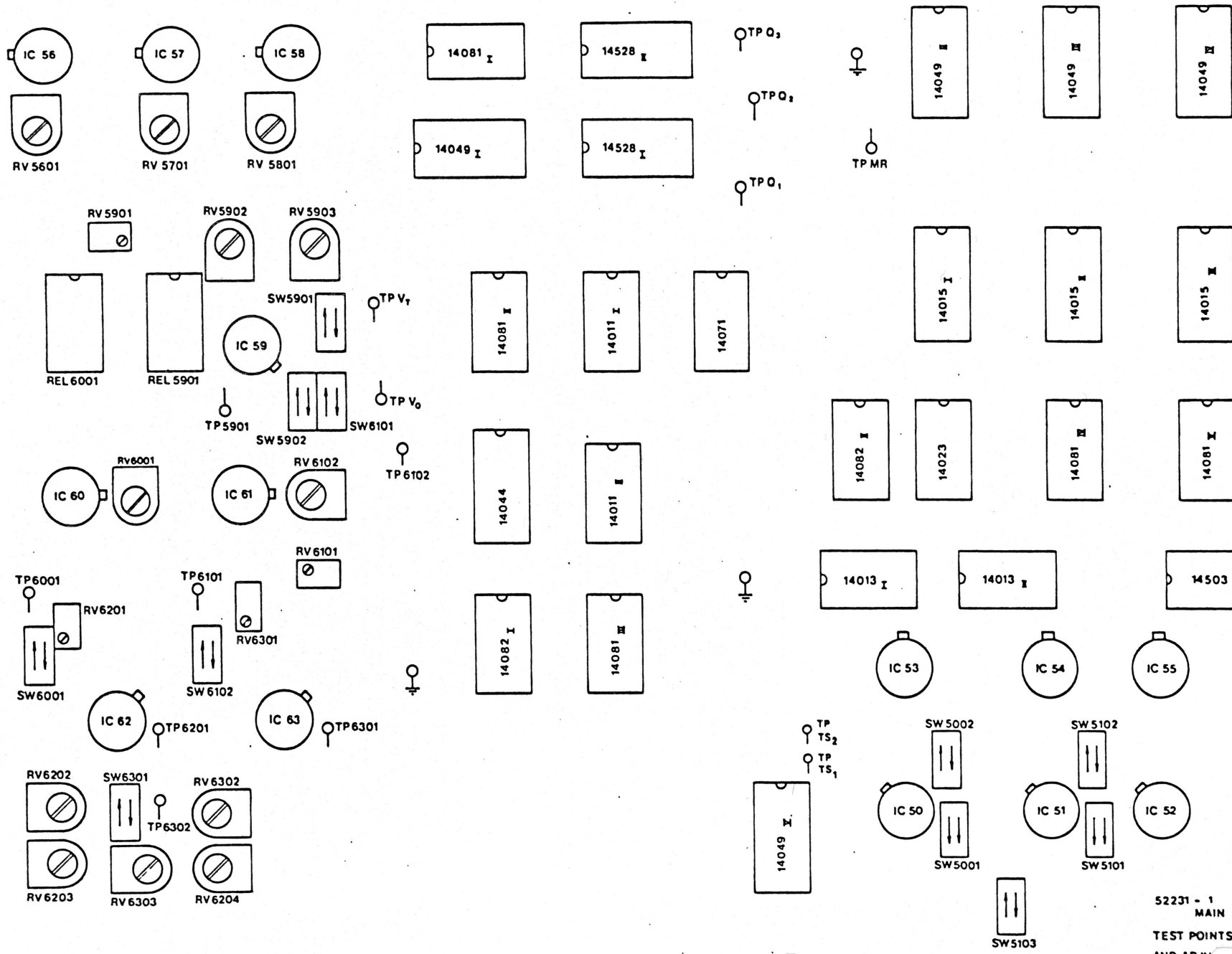


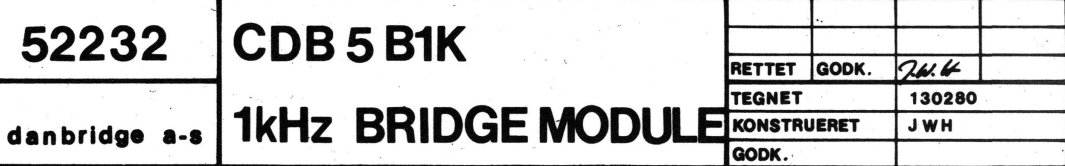


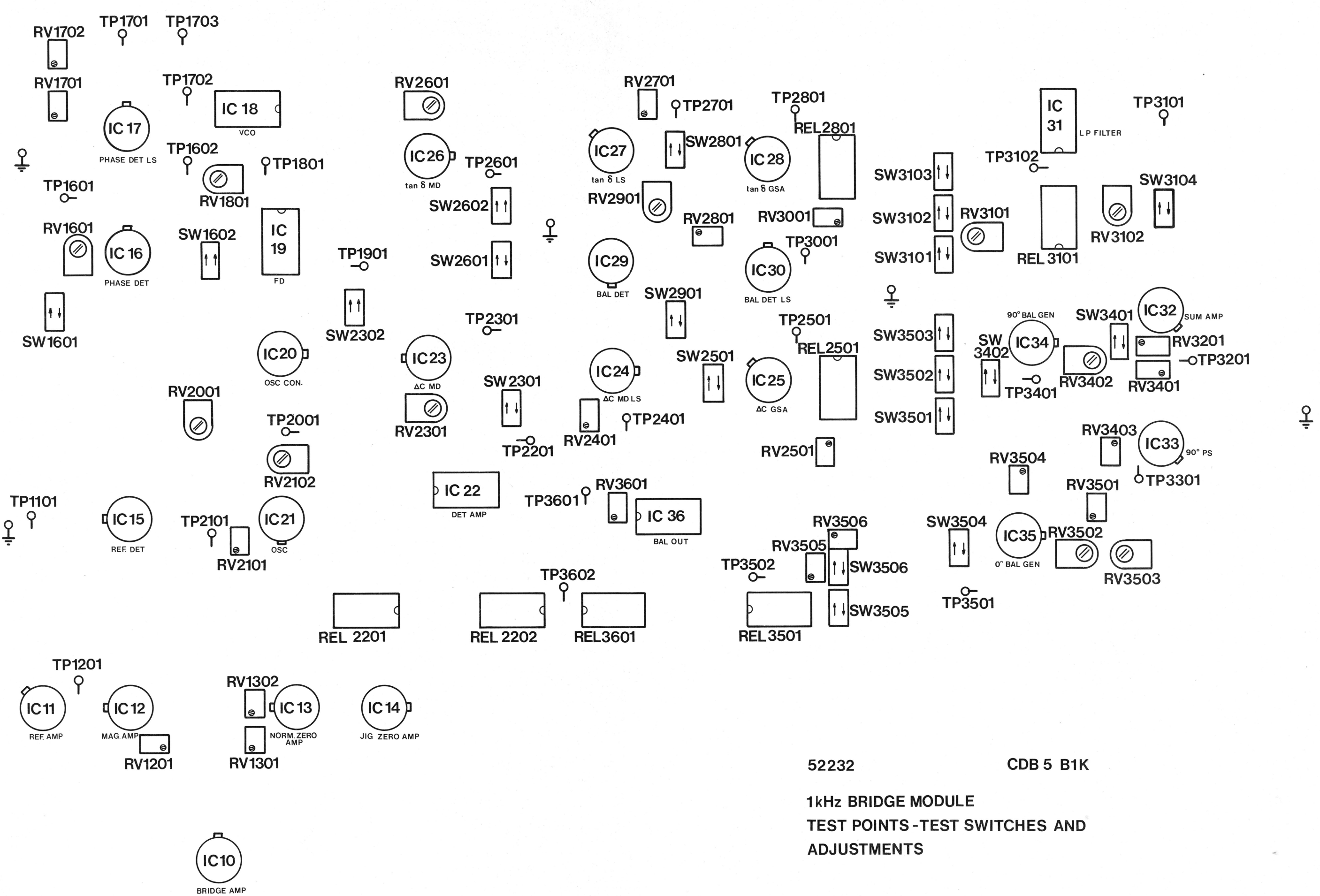
**CDB 5    52231**











52232

CDB 5 B1K

1kHz BRIDGE MODULE  
TEST POINTS - TEST SWITCHES AND  
ADJUSTMENTS

DANBRIDGE A-S

KONSTR.: JWH  
TEGN.: B.RAS



